

Date Created : 2009/07/05  
Date Issued On : 2009/08/10  
PCN# : Q3092702

DESIGN/PROCESS CHANGE NOTIFICATION -- FINAL

This is to inform you that a design and/or process change will be made to the following product(s). This notification is for your information and concurrence.

If you require data or samples to qualify this change, please contact **Fairchild Semiconductor within 30 days of receipt of this notification.**

Updated process quality documentation, such as FMEAs and Control Plans, are available for viewing upon request.

If you have any questions concerning this change, please contact:

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Implementation of change:  
Expected 1st Device Shipment Date: 2009/11/16

Earliest Year/Work Week of Changed Product: 0947

Change Type Description: Alternate Assembly/Test Location/Qualification

Description of Change (From): KSC5502DTM is currently manufactured at SP Semiconductor & Communication Co Ltd. located in Korea with package outline dimensions that do not fully conform to the JEDEC requirement.

Description of Change (To): KSC5502DTM will be manufactured at Fairchild Semiconductor located in Suzhou, China with package outline dimensions that will conform to JEDEC requirement.

Reason for Change : Qualify Fairchild's Suzhou manufacturing site to improve capacity and flexibility. This change will not affect any electrical characteristics or reliability performance.

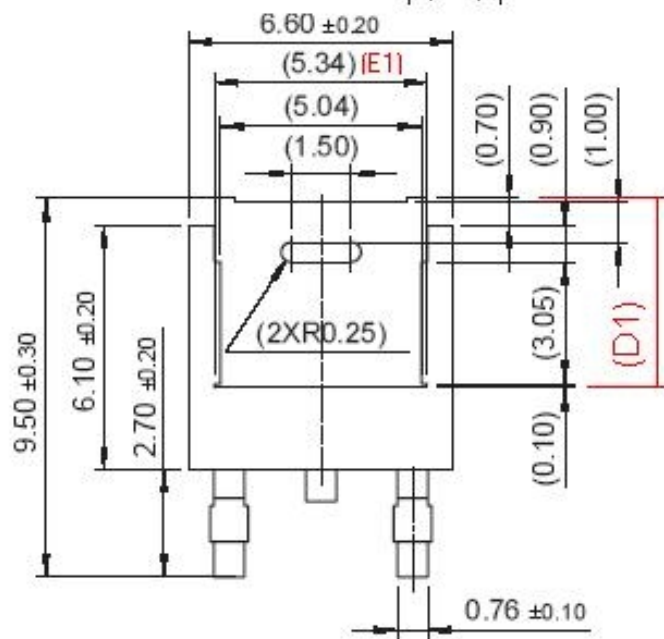
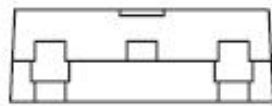
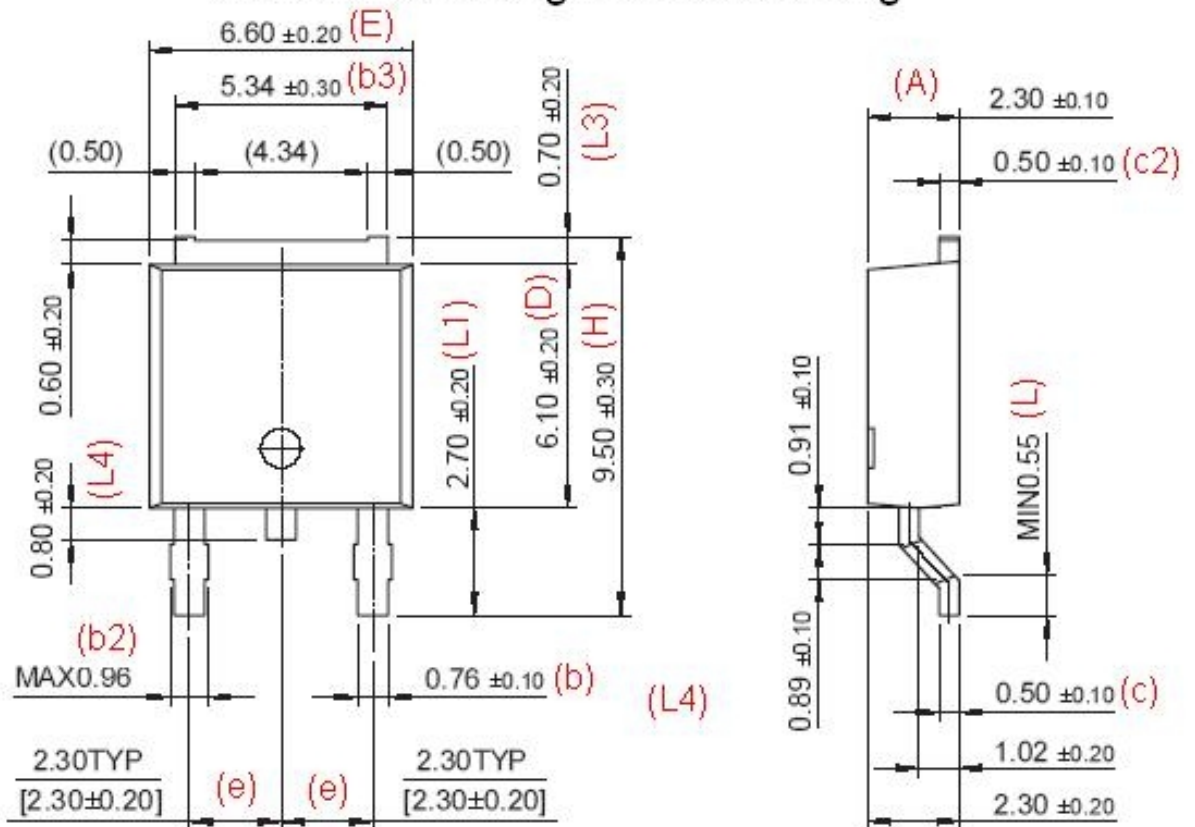
Qual/REL Plan Numbers : Q20090404

Qualification :

Passed and met Fairchild reliability qualification requirement.

Change From

# DPAK (FS PKG CODE AA) Current Marketing Outline Drawing



Dimensions in Millimeters

Change To

**A) Physical Dimension Comparison**

- DPAK

	DPAK (New type)		DPAK (Current)		Jedec AA		
	Min	Max	Min	Max	Min	Nom	Max
A	2.275	2.325	2.20	2.40	2.184	-	2.388
A1	-0.012	0.038	-	-	-	-	0.127
b	0.740	0.840	0.66	0.86	0.635	-	0.889
b2	0.800	1.000	-	0.96	0.762	-	1.143
b3	5.310	5.410	5.04	5.64	4.953	-	5.461
c	0.508	0.558	0.40	0.60	0.457	-	0.610
c2	0.508	0.558	0.40	0.60	0.457	-	0.889
D	6.075	6.125	5.90	6.30	5.969	6.096	6.223
D1	5.235	5.385	4.75 Ref		5.207	-	-
E	6.515	6.565	6.40	6.80	6.350	-	6.731
E1	4.730	4.830	5.34 Ref		4.318	-	-
e	2.286 BSC		2.30 BSC		2.286 BSC		
H	9.925	10.275	9.20	9.80	9.398	-	10.414
L	1.400	1.700	0.55	-	1.397	1.524	1.778
L1	2.700	2.900	2.50	2.90	2.743 Ref		
L3	1.150	1.250	0.50	0.90	0.889	-	1.270
L4	0.740	0.940	0.60	1.00	-	-	1.016

**B) Bill of Material Comparison**

Process	Current SUBCON	New SUZHOU
Technology	Transistor	Transistor
Molding Compound	KTMC-5400SM (KCC)	EME-6600CS4L (Sumitomo)
Solder Wire Composition	93.5Pb5Sn1.5Ag	92.5Pb5Sn2.5Ag
Bonding wire material	Al wire	Al wire
Lead Finish	Matte Sn	Matte Sn
Lead Frame	Base Material: PMC90 (PoongSan, Korea), 12SnOFC (Hitachi) Supplier: TSP/Shinwon/STW	Base Material: 12SnOFC (Hitachi) Supplier: TSP
Lead Frame Plating	Pad Plating – Bare Cu Post Plating – Ni	Pad Plating – Bare Cu Post Plating – Ni

**Results/Discussion for Qual Plan Number Q20090404**

Test: (Autoclave)   Conditions: 100%RH, 121C   Standard: JESD22-A102					
Lot	Device	96-HOURS	Failure Code		
Q20090404AAACL	KSC5502DTM	0/77			

Test: (High Humidity, High Temp, Rev. Bias)   Conditions: 85%RH, 85C, 80% of Rated BV   Standard: JESD22-A101B					
Lot	Device	168-HOURS	500-HOURS	1000-HOURS	Failure Code
Q20090404AAH3TRB	KSC5502DTM	0/77			
			0/77		
				0/77	

Test: (High Temperature Reverse Bias)   Conditions: 150C, 80% Rated BV   Standard: JESD22-A108					
Lot	Device	168-HOURS	500-HOURS	1000-HOURS	Failure Code
Q20090404AAHTRB		0/77			
			0/77		
				0/77	

Test: (Precondition)   Conditions:   Standard: JESD22-A113			
Lot	Device	Results	Failure Code
Q20090404AAPCNL2A	KSC5502DTM	0/231	

Test: (Temperature Cycle)   Conditions: -65C, 150C   Standard: JESD22-A104				
Lot	Device	200-CYCLES	500-CYCLES	Failure Code
Q20090404AATMCL1	KSC5502DTM	0/77		

Q20090404AATMCL1	KSC5502DTM		0/77	
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Product Id Description :

Affected FSIDs :

KSC5502DTM		
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