



Date Created: 12/30/2003
Date Issued: 2/2/2004
PCN # 20040001

FORECAST CHANGE NOTIFICATION

This is to inform you that a design and/or process change will be made to the following product(s). This notification is for your information and concurrence. This is a preliminary notification. A final PCN will be issued when qualification is complete and data is available.

If you require data or samples to qualify this change, please contact **Fairchild Semiconductor within 30 days of receipt of this notification.**

If you have any questions concerning this change, please contact:

Name: Rivero, Doug M.
E-Mail: Doug.Rivero@notes.fairchildsemi.com
Phone: 1-408-822-2143

PCN Originator

Name: Knapp, Paul E.
E-mail: Paul.Knapp@notes.fairchildsemi.com
Phone: 408-822-2133

REL Engineer

Name: Uy, Lester O.
E-mail: Lester.Uy@notes.fairchildsemi.com
Phone: 63-32-3415636

PCN Type: Bump Process/Method

Effectivity

Expected 1st Device Shipment Date: 5/3/2004
Earliest Year/Work Week of Changed Product: 0419
(Note: Package marking may differ from this format)

Product ID (Description):

This change will affect Power Discrete products assembled in the various BGA packages. The products affected by this change are listed below in the "Affected FSIDs" section.

Description of Change:

As part of Fairchild Semiconductor ongoing effort to increase its manufacturing capacity for various products in our various BGA packages, we intend to qualify an internal lead free bump process from a high lead process performed by an external foundry.

Effect of Change:

This change will have no impact on any of the electrical parameters of the products involved. The product test conditions, test limits, and performance will remain unchanged. Summary of the changes follows.

BGA products

Process	Current - High Lead Bump	New - Lead Free Bump
Bump	95% Pb-5%Sn ball w/UBM	99.99% 3mil Pd coated Cu wire w a SnAgCu solder bump
Passivation	SiON and BCB (Benzocyclobutene)	SiON - no change in SiON thickness

Qualification:

The qualification of this change will consist of key silicon vehicles. See qual plan for details.

Qual/REL Plan Numbers

Additional Qualification Data
Qual Plan # : QP03500127- E

Qualification Vehicle

Device	Bump Size (um)	Array Size (mm)	VDS/VGS Rating
FDZ206P	300	4.0X3.5	20/12

QUALIFICATION REQUIREMENTS

A) RELIABILITY TESTS, COMPONENT LEVEL

TEST DESCRIPTION/CONDITION	REL LOCATION/ Applicability	DURATION	NBR OF LOTS	SAMPLE SIZE	ACC/REJ
ACLV @ 121 °C, 15psi, 100% RH with 3 X IR re-flow at 250 C	FSCP	96 Hrs	3	79	0/1
TMCL @ -65 C to 150 C, 30 min/ cycles with 3 X IR re-flow at 250 C	FSCP	100, 500 cycles	3	79	0/1
HAST @ 130 C, 85 % RH 80% of Rated BV, with 3 X IR re-flow at 250 C	FSCP	96 Hrs	3	79	0/1
PRCL @ 125°C T _{JC} , delta T _j of 100 C, 2 min on, 2 min off	FSCP	5k,10k	3	79	0/1
HTRB @ 80% of Rated BV, 150 deg C	FSCP	168, 500, 1k hrs	3	79	0/1
HTGB @ 100 % Rated VGS, 150 deg C	FSCP	168, 500, 1k hrs	3	79	0/1

B). RELIABILITY TESTS, BOARD LEVEL (Solder Joint Reliability)

TEST DESCRIPTION/ CONDITION	LOCATION	DURATION	NBR OF LOTS	SAMPLE SIZE	ACC/REJ
-10 to 100 deg C, 30 minutes per cycle with 2 pass IR re-flow at 250 C prior to boardmount	FSCP	63% failure rate or stop at 2500 cycles if no failure is seen	3	79	N/A

Affected FSIDs

FDZ201N	FDZ202P	FDZ203N
FDZ204P	FDZ206P	FDZ208P
FDZ209N	FDZ2551N	FDZ2552P
FDZ2553N	FDZ2553NZ	FDZ2554P
FDZ2554PZ	FDZ298N	FDZ299P
FDZ5047N	FDZ7064N	FDZ7064S