

Application Note 42037

ML4423 Application Guidelines

INTRODUCTION

Depending on the application, the focus of a given motor control design can fall on one of many specific parameters. Different applications may require that special attention be given to a specific control method to guarantee the desired performance. This Application Note defines and clarifies industry terminology for these control parameters, and will assist in utilizing the ML4423 for many different AC motor control applications.

3rd HARMONIC INJECTION

A review of basic inverter output waveforms will help introduce the concept of the 3rd harmonic injection.

When 3-phase, 120 degree sinusoidal voltage PWM waveforms are supplied to the power inverter H and L inputs (Figure 1), the integrated PWM phase output waveforms will look like Figure 2 (phase C has been omitted for clarity).

For this discussion, V_{BUS} is equal to the relative amplitude of 1.0. The V_{BUS} ground (GND) will be referenced to the relative amplitude of -1.0. This constrains the peak value of the phase waveforms (Figure 2) to the maximum value of ± 1.0 (for unclipped sinusoidal waveforms). So, when the differential waveform is at its positive peak, (Figure 2, point B) the Q1 switch is modulating near V_{BUS} and the Q4 switch is modulating near GND (Figure 1). When the differential waveform is at its negative peak, the Q3 switch is modulating near V_{BUS} and the Q2 switch is modulating near GND. In this instance, neither phase amplitude (Figure 2, point A) is at its peak value when the differential amplitude is at its peak value (Figure 2, point B). For this condition, V_{BUS} is not being fully utilized. The differential amplitude is $\sqrt{3} \times V_{PHASE}$. The differential amplitude peaks when the phase amplitude is at 0.865 of its maximum. For a sinusoidal waveform, the bus voltage required is expressed in this formula:

$$V_{BUS} = V_{DIFFRMS} \times \frac{\sqrt{2}}{0.865} \quad (1)$$

Reordering to solve for $V_{DIFFRMS}$:

$$V_{DIFFRMS} = V_{BUS} \times 0.612$$

Figure 3 shows a phase voltage waveform and its 3rd harmonic. When the 3rd harmonic is summed with the phase waveform, a new 3rd harmonic+phase waveform is created. The amplitude of the 3rd harmonic signal has been equalized slightly to maintain a peak value of 1.0 in the resulting 3rd harmonic+phase waveform.

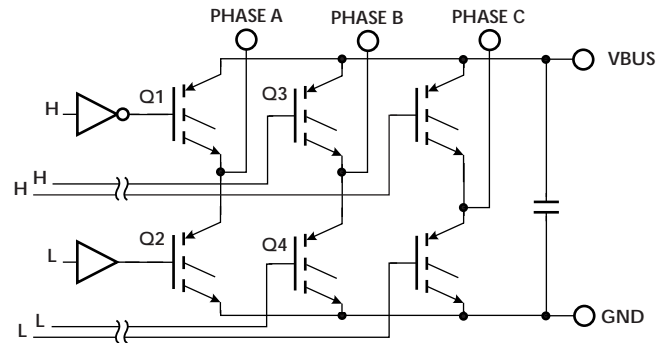


Figure 1. Power Inverter

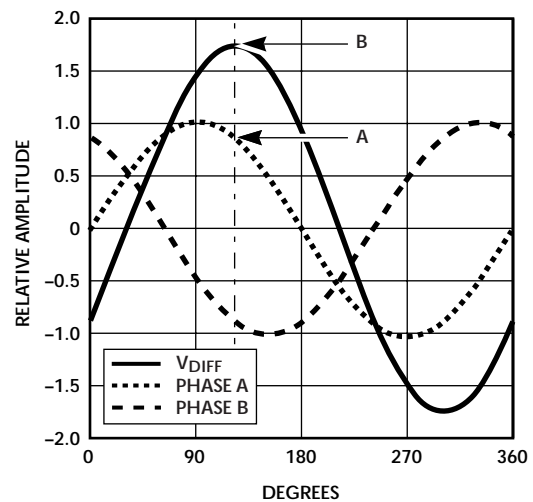


Figure 2. Sinusoidal Waveforms

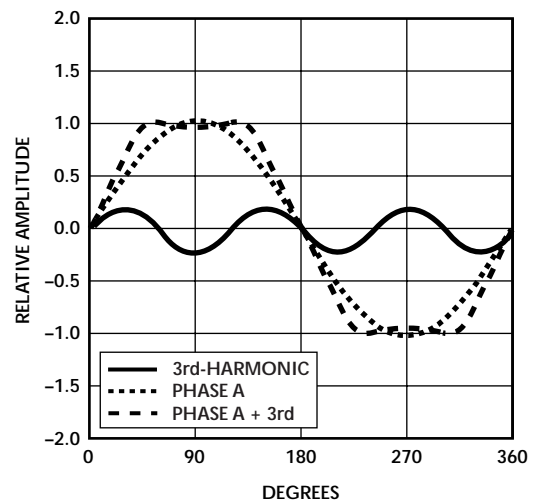


Figure 3. Creating 3rd Harmonic Waveform

Application Note 67

3rd HARMONIC INJECTION (Continued)

Figure 4 shows two output phase waveforms with their 3rd harmonics added, and the resulting differential waveform. When the differential waveform is at its positive peak, the Q1 switch is at V_{BUS} and the Q4 switch is at GND (Figure 1). When the differential waveform is at its negative peak the Q3 switch is at V_{BUS} and the Q2 switch is at GND. The peak differential amplitude is $\pm V_{BUS}$. Since the differential waveform is higher in amplitude than in Figure 2, a new equation is used to derive V_{BUS} . The equation is:

$$V_{BUS} = V_{DIFFRMS} \times \sqrt{2} \quad (2)$$

$$V_{BUS} = 220 \times \sqrt{2} = 311V$$

It should also be noted that:

$$V_{DIFF(PEAK)} = V_{DIFFRMS} \times \sqrt{2}$$

$$V_{DIFF(PEAK)} = 220 \times \sqrt{2} = 311V$$

The ML4423 can be configured to provide similar results. Slight clipping will occur with the ML4423, because the phase voltages are trapezoidal in nature (when V_{SPEED} is at 4.4V). Note that the 3rd harmonic phase waveforms have dips in the center (Figure 3). This slight dip keeps the differential waveform from saturating near its peak amplitude. For this case V_{BUS} is fully utilized. Using the ML4423 in this way allows:

$$V_{DIFFRMS} = \frac{V_{BUS}}{\sqrt{2}} \quad (3)$$

CONFIGURING THE ML4423

To configure the ML4423 for pseudo-3rd harmonic injection, determine the value of V_{BUS} to satisfy the following parameters:

- $V_{SPEED} = 4.4V$
- $V_{SINEREF} @ 1V_{RMS} \times \sqrt{2}, = 1.5V$ peak
- $V_{MOTOR} = 220V_{RMS}$

To find $SENSE_A$, $SENSE_B$, $SENSE_C$ feedback divider ratio, the desired output voltage is configured as indicated (see Figure 5):

$$V_{MOTOR(PEAK)} = \left(\frac{R1 + R2}{R2} \right) \times V_{SINE(PEAK)} \quad (4)$$

Solving for R1:

$$R1 = \left(\frac{V_{MOTOR(PEAK)} \times R2}{V_{SINE(PEAK)}} \right) - R2$$

$$R1 = \left(\frac{311V \times 1000\Omega}{1.5V} \right) - 1000\Omega = 206.3k\Omega$$

Total harmonic distortion of 6% is shown in Figure 6.

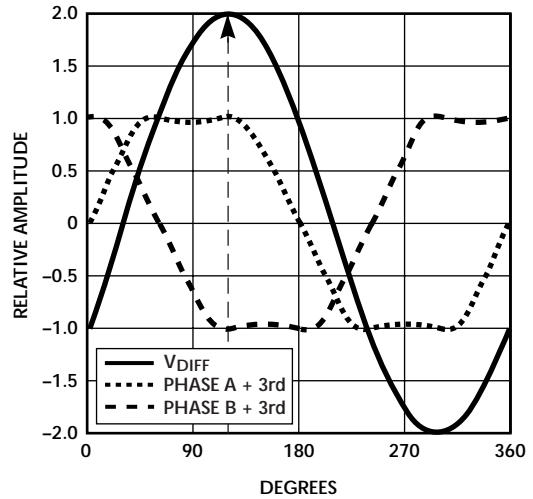


Figure 4. 3rd Harmonic Waveforms

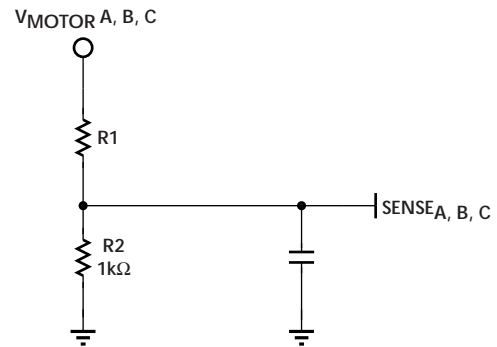


Figure 5. R1/R2 Divider

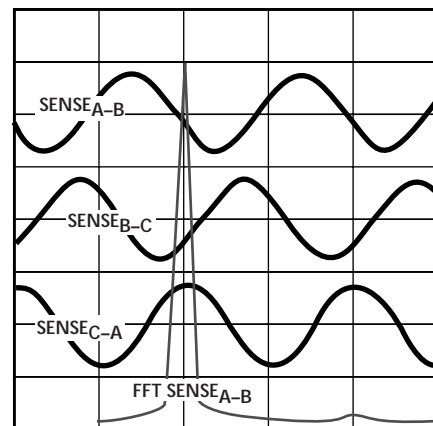


Figure 6. Fast Fourier Transform of Sense A-B Waveforms

DC INJECTION BRAKING

DC injection braking works on the principle that if a DC current is imposed on the motor windings, the resulting stationary flux will cause the rotor to slow.

To utilize DC injection braking (Figure 7), provide a high signal on the DC brake, which will cause Q3 to pull the $\overline{\text{COAST}}$ signal low, and will briefly disable the output PWM. The $\overline{\text{COAST}}$ signal low state will remain for the time period set by the RC network of a $1\mu\text{F}$ capacitor and a $100\text{k}\Omega$ resistor. At the same time Q2 will pull the V_{SPEED} signal to 0V. Next, Q1 raises the voltage on the V_{MIN} signal. Then Q3 releases the $\overline{\text{COAST}}$ signal after the RC network discharges and the PWM comes back on. At that time the motor will receive a near DC current to each winding for the time period set by the RC network of a $5\mu\text{F}$ capacitor and a $1\text{M}\Omega$ resistor. When the RC time

expires the V_{MIN} signal will return to its original setting and the PWM will remain on. The values given should be adequate for a preliminary design.

This technique forces the motor to slow down much faster than coasting. With regenerative schemes, a load dissipater, an added switch, and some support circuitry would be required. No overvoltage will develop at the inverter since the slip on the motor will be large during braking.

SOFT START

Increasing the capacitance on the V_{SPEED} signal would allow a soft start to occur when the DC brake signal is pulled low.

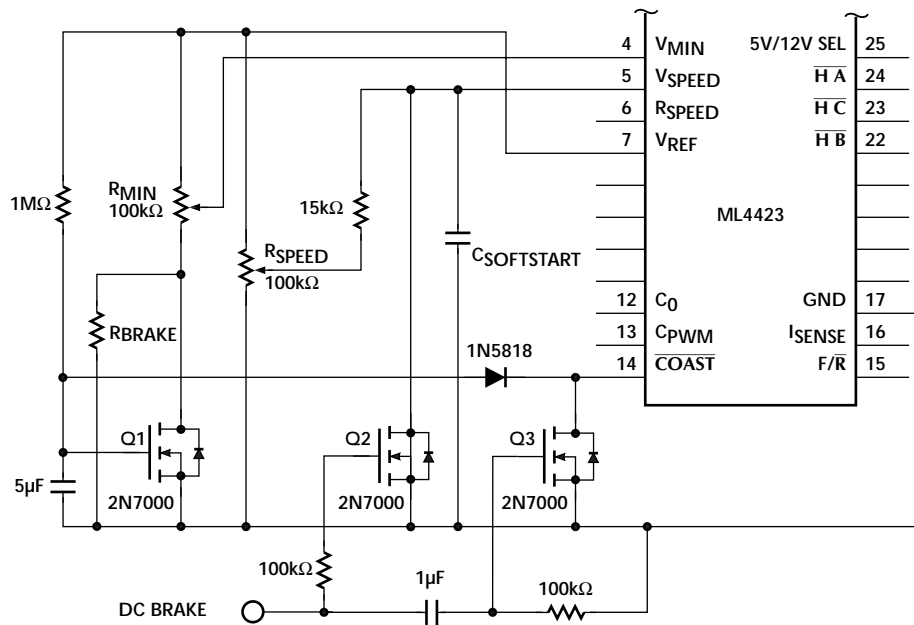


Figure 7. DC Braking Circuit

LOOP CHARACTERISTICS (Continued)

FEEDBACK GAIN VS. FREQUENCY

The internal GM amplifiers can operate with no bypass capacitors. In some cases it may be necessary to lower the loop gain to reduce the feedback bandwidth and eliminate subharmonic oscillations. The GM amplifiers have a high open loop gain, and with capacitance on the GM1 and GM2 outputs, the gain can be tailored to rolloff at predicted frequencies. Figures 12 through 17 are examples of gain vs. frequency for the given capacitance.

SPEED LOOP

Closing a speed loop using the ML4423 can be done by using a shaft speed sensor. The sensor generates an error signal, which is used to close a loop around a reference speed signal, and is then fed into the ML4423 speed input pin (Figure 18).

There are additional benefits when using the slip control loop, which enables the motor slip to be set to a valve. When the motor accelerates, the motor current is limited to the value set by the slip control circuit. This ensures that the motor will accelerate at a predetermined rate, and will operate within the current limit of the ML4423.

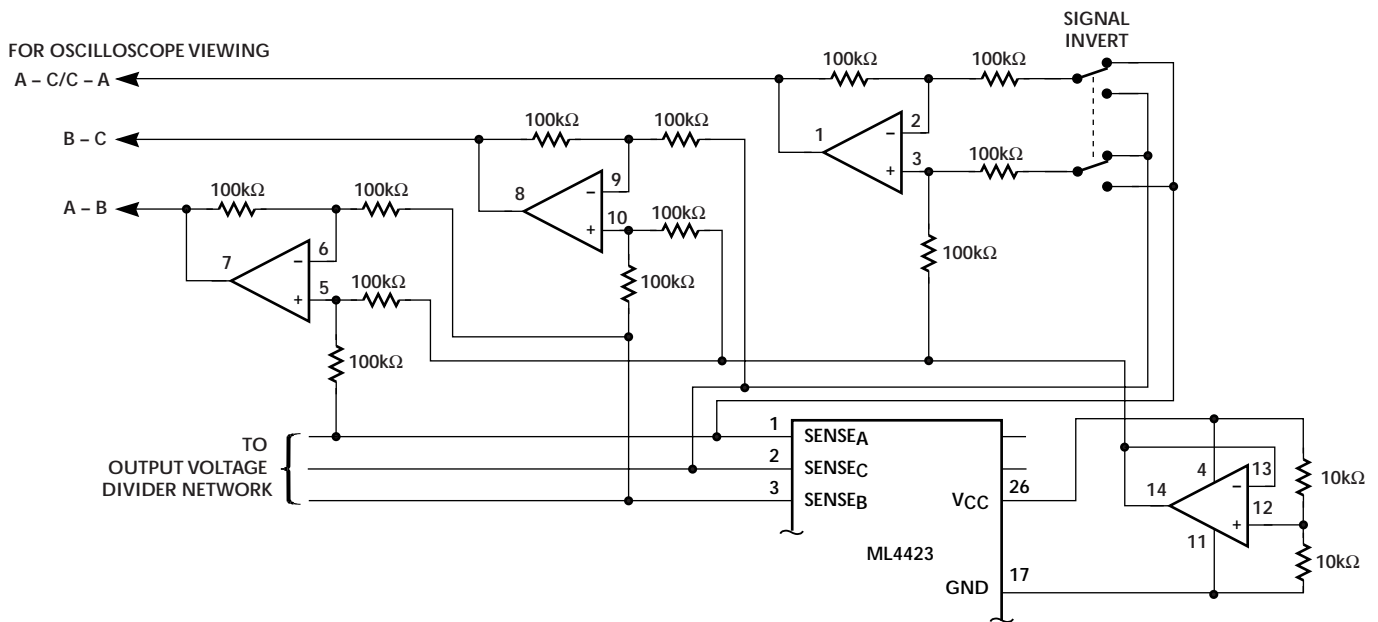


Figure 9. Differential Observer Circuit

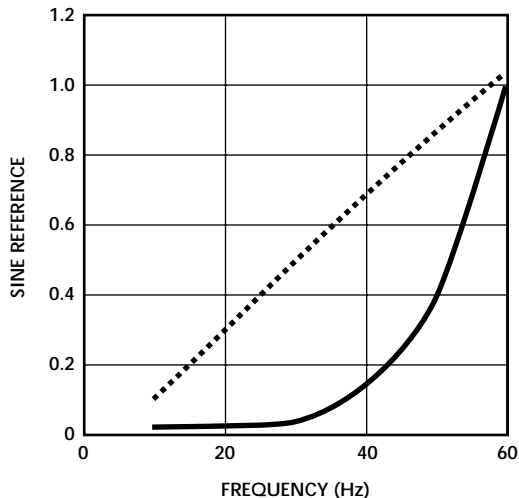


Figure 10. Linear and Exponential V/F

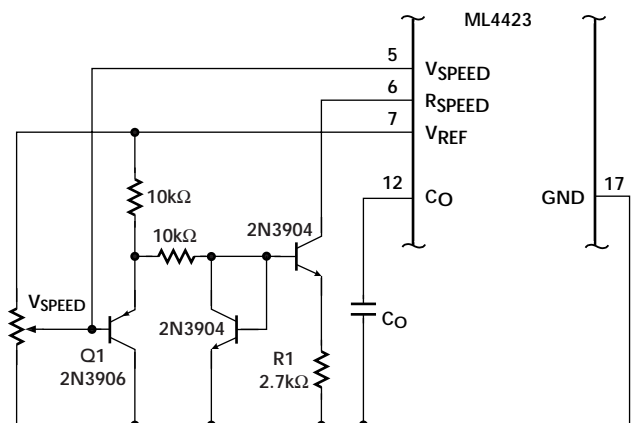


Figure 11. Current Sink Circuit

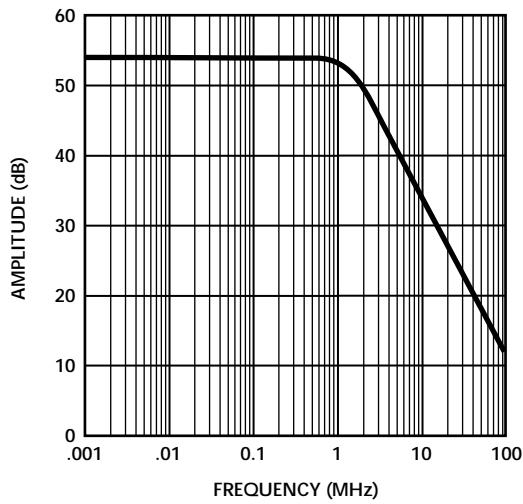


Figure 12. Bode Plot with no Capacitor

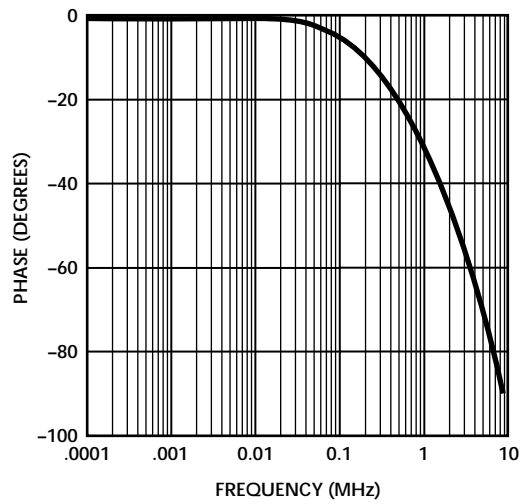


Figure 13. Phase Response with no Capacitor

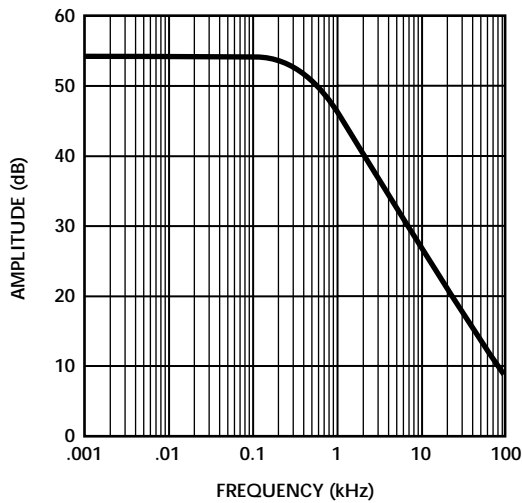


Figure 14. Bode Plot with a 1nF Capacitor

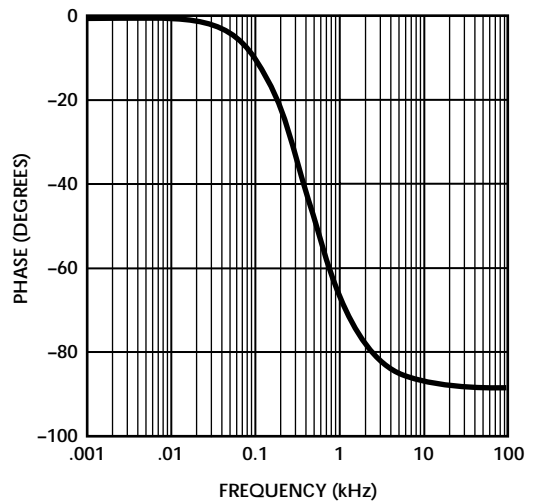


Figure 15. Phase Response with a 1nF Capacitor

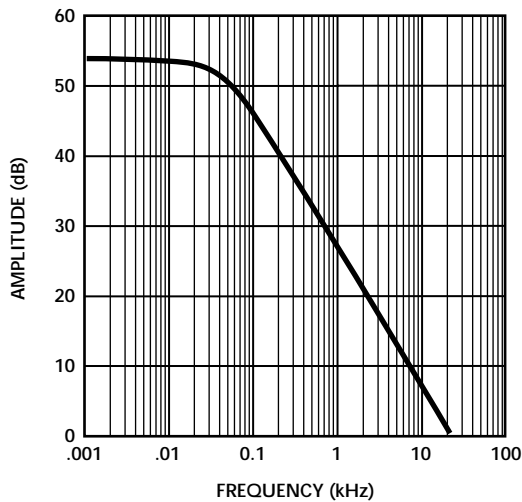


Figure 16. Bode Plot with a 10nF Capacitor

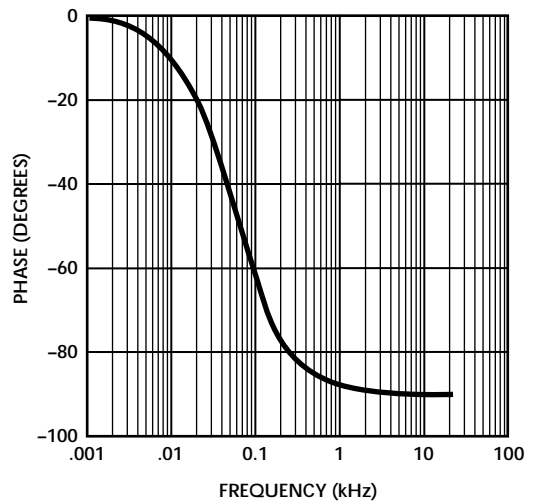


Figure 17. Phase Response with a 10nF Capacitor

Application Note 67

OFFLINE OPERATION

Offline bias circuits can range from the leaky cap style to low cost 120V to 12V AC transformers (Figure 19). The transformer does offer isolation, but the power stage coupled to the line defeats it, since R_{SENSE} provides a connection to the AC return. Fast rising and falling noise spikes coupled on the 12V supply will ruin a good PCB layout. The ML4423 and inverter bootstrap circuitry typically consume 50mA at 12V DC.

OFF-LINE APPLICATIONS

A simple voltage doubler circuit will raise the 110V line to about 325VDC. This allows operation with 115V motors with sufficient headroom in the closed loop mode. In open loop mode the bus voltage determines the motor voltage. The capacitor RMS ripple current is equal to $I_{SENSE} / \sqrt{2} / \sqrt{3}$.

SINGLE & TWO-PHASE OPERATION

The ML4423 can be used to operate single-phase motors. The IC would drive the appropriate gate buffers and H bridge transistors. The ML4423 HA, LA, HC, LC, $SENSE_A$, and $SENSE_C$ pins would provide the necessary I/O functions. $SENSE_B$ input would be grounded, and the motor voltage would be fed back from phase A to $SENSE_A$ and phase C to $SENSE_C$ with a resistive divider network. The two phase mode is selected.

For the two-phase mode, the component count required is the same as for the three phase mode inverter configuration. The main motor winding is connected to A and C inverter outputs and the secondary motor winding is connected to B inverter output. The two phase mode is selected. The ML4423 contains no boost feature on the secondary winding, which is required for some two phase motors to produce adequate starting torque.

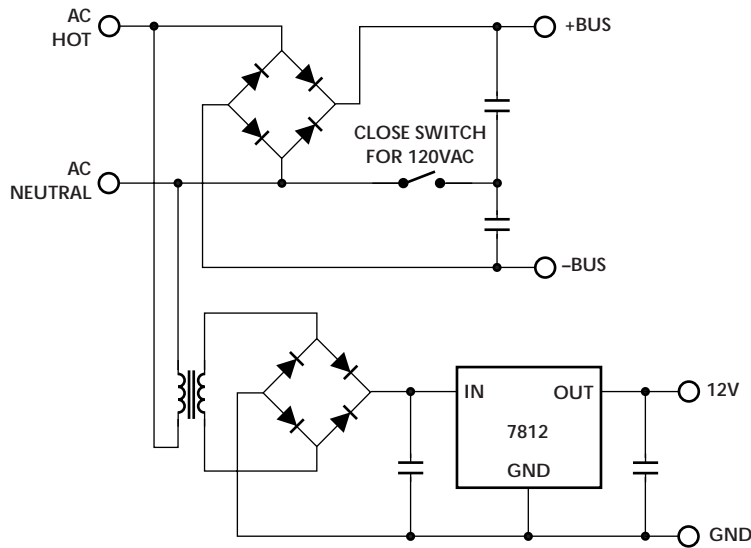


Figure 19. Low Cost 12V AC Transformer/120V Boost

LAYOUT CONSTRAINTS

Figure 20 shows the current loop areas relating to circuit layout and function. Critical loop areas are:

- Diode recovery
- Gate drives
- Bootstrap charging
- Motor di/dt

Since the current sense resistor is utilized by three of the four loops, it needs to be a low inductance type. Diode recovery currents are diverted from the current sense resistor by the film capacitor, since the peak recovery currents can be higher than the actual motor current. This would prematurely trip the current limit.

The film capacitor should have sufficient energy storage to handle the diode recovery time. An R/C filter on the I_{SENSE} pin is needed to filter any spikes. Typical values range from 330pF to 1nF (R = 1kΩ). Minor loops not highlighted include the voltage and current feedback paths to the ML4423.

The PCB layout itself can make or break a successful design. Circuit layouts without these considerations will operate erratically under load, and may cause the output power stage, gate drivers, and/or ML4423 to fail. The PCB design examples on the following pages reflect loop area control.

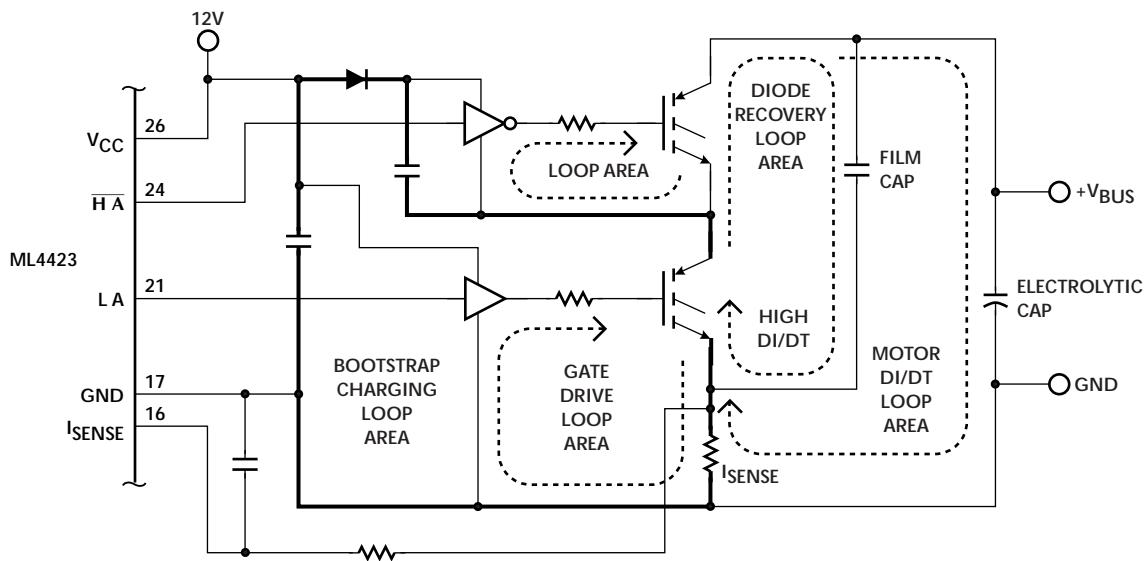


Figure 20. Current Loops

LAYOUT CONSTRAINTS (Continued)

THROUGH-HOLE PCB EXAMPLE

The ML4423 through-hole PCB in Figures 21a through 21f illustrates the use of a ground plane. A single sided layout should never be attempted. This is because of the possibility of ground bounce. Whenever ground referenced sensing is used the ground itself must be stable and low in noise. Single layer boards can't satisfy this requirement since the gradients, or differences, in voltages occur at different points on the board due to stray inductance. The voltage differences in ground traces creates voltage differences at the control IC. The C_O pin on the ML4423 is susceptible to any form of noise because of its low amplitude of 300mV_{p-p}. Therefore, proper layout is essential for reliable circuit operation. The most straightforward solution is a separate ground plane. This layer, either as the top or bottom layer of the PCB, reduces the gradient voltage effect across the PCB. The stray inductance is also reduced since the trace currents are mirrored on the ground plane. A possible difficulty occurs when a power inverter has to occupy the same PCB as the control IC. In this case, the phase

output tabs, upper gate drivers, and output voltage feedback resistors should have clearance away from the ground plane to reduce the opportunity of high frequency combined with high voltage switching transients being coupled by capacitance into the ground plane (see the ML44xx PCB layout).

SURFACE MOUNT PCB EXAMPLE

The surface mount PCB in Figures 22a through 22i follows the listed guidelines. The control IC has a ground plane and is a combination surface mount and through-hole. The power inverter does not have an active ground plane, but uses parallel traces to reduce loop area, uses surface mount devices, and uses the isolation of the FR-4 material for its dielectric withstand capability. The bus power PCB has the plus and minus bus on opposite sides, near critical power transistor collector/emitter connections, reducing the stray inductance loop area. The ground loops are managed locally, then connected together by traces. This assembly controls motors to 1/2HP with a suitable heatsink.

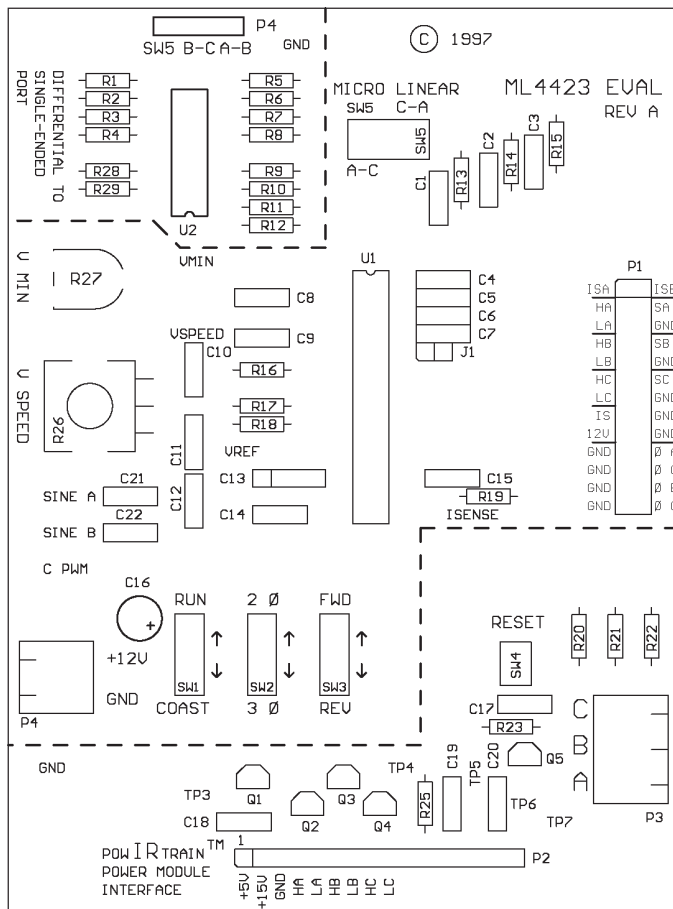


Figure 21a. ML4423 Silkscreen

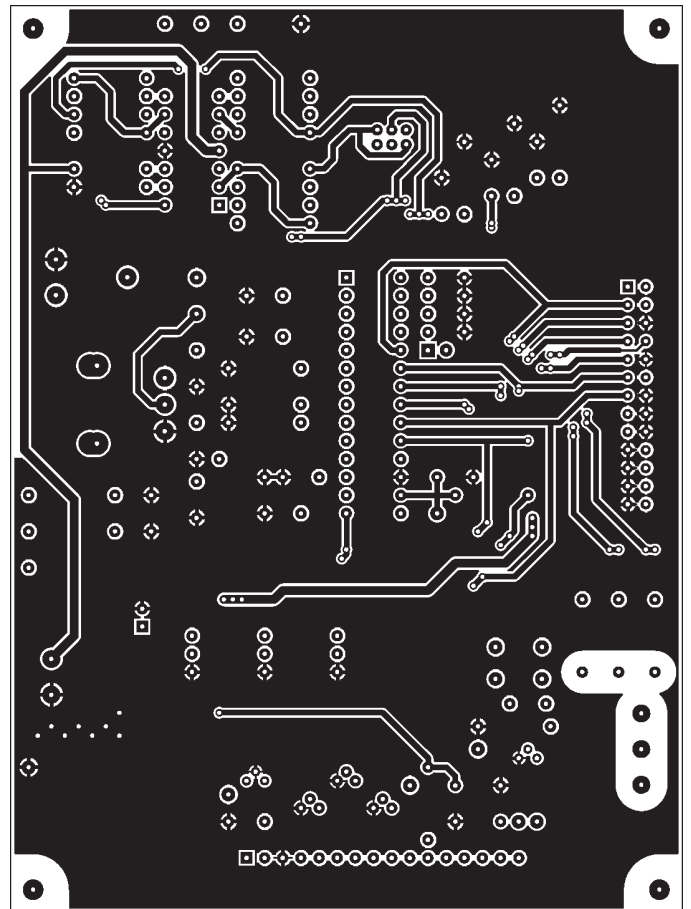


Figure 21b. ML4423 Top Layer

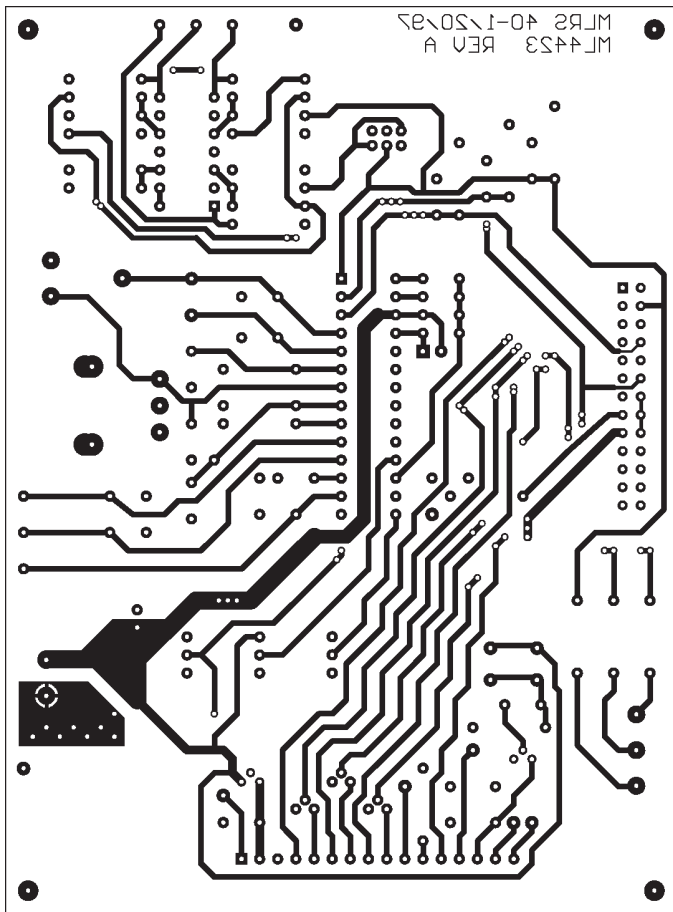


Figure 21c. ML4423 Bottom Layer

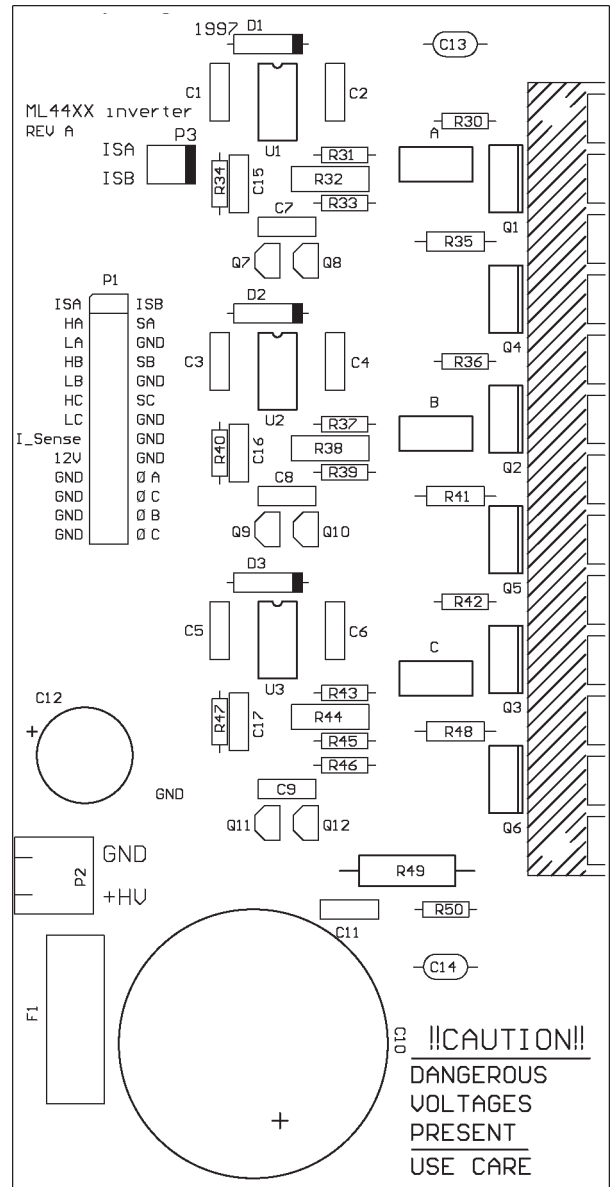


Figure 21d. ML44xx Silkscreen

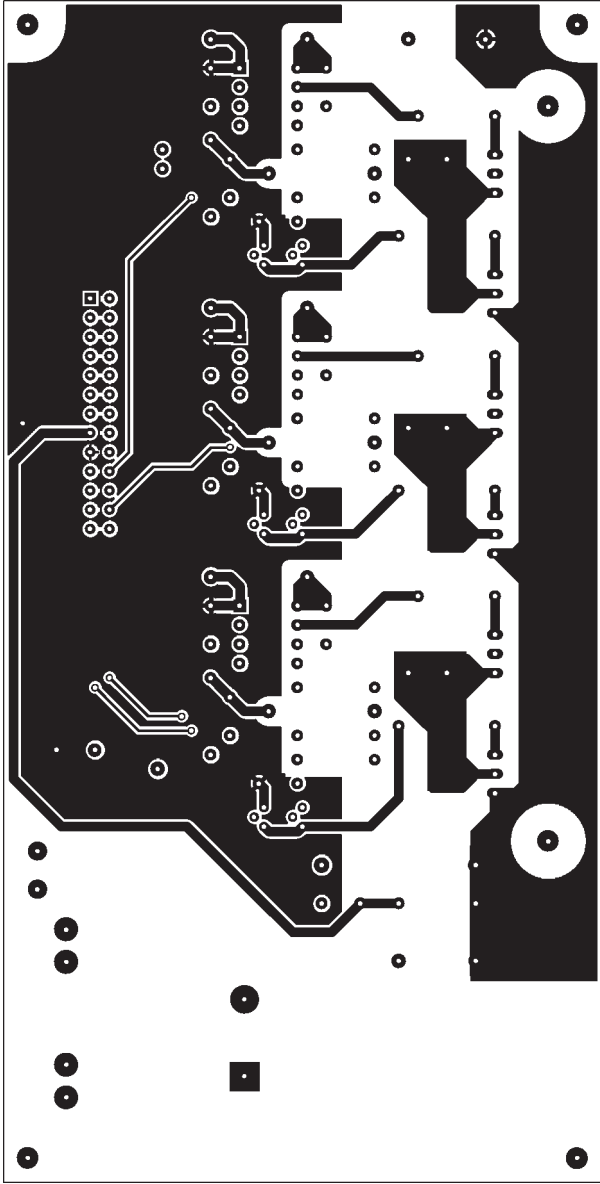


Figure 21e. ML44xx Top Layer

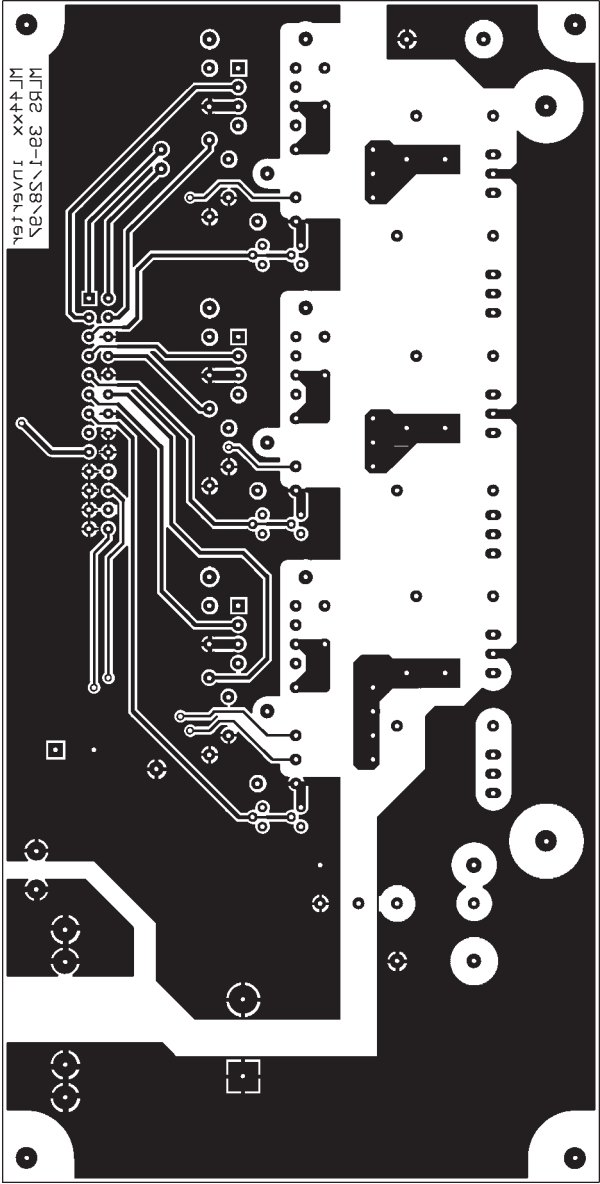


Figure 21f. ML44xx Bottom Layer

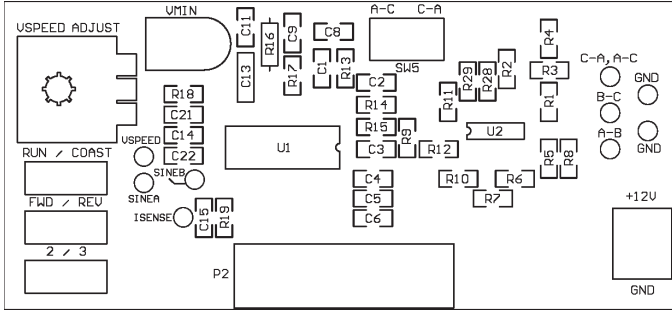


Figure 22a. Control PCB Silkscreen

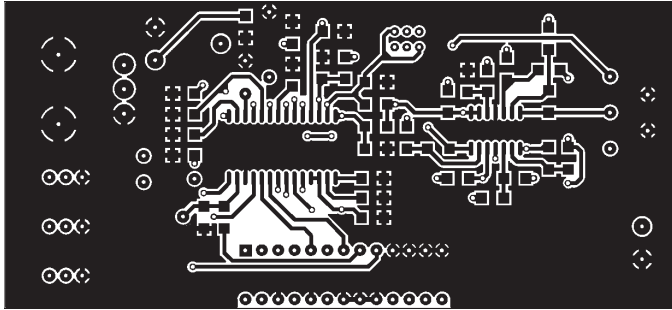


Figure 22b. Control PCB Top Layer

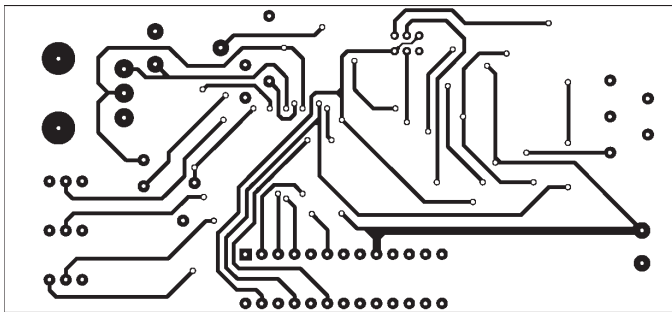


Figure 22c. Control PCB Bottom Layer

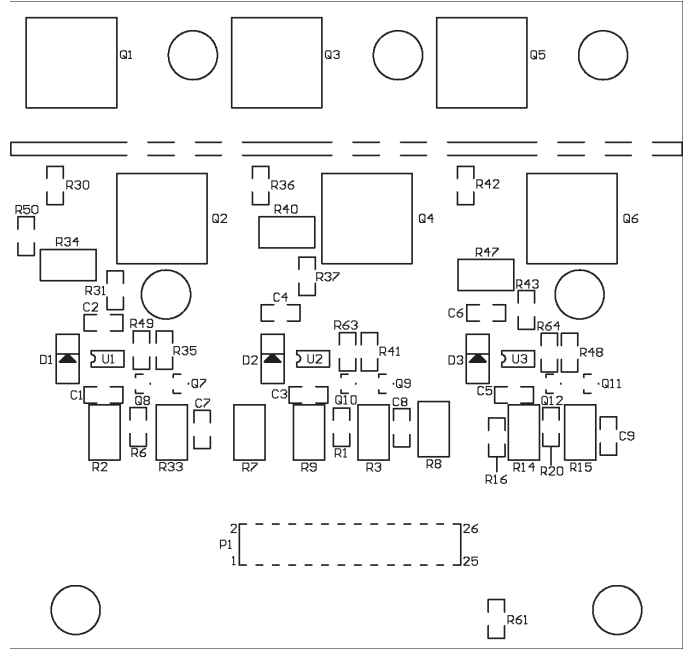


Figure 22d. Power PCB Silkscreen

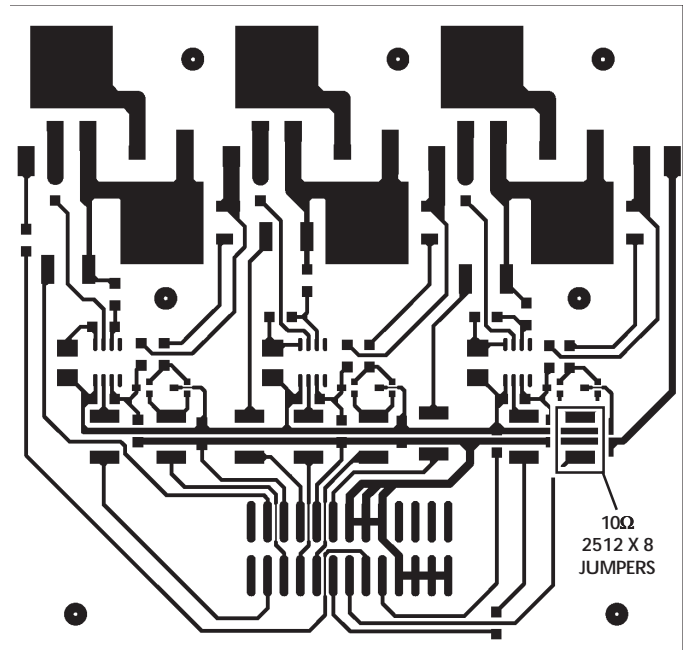


Figure 22e. Power PCB Top Layer

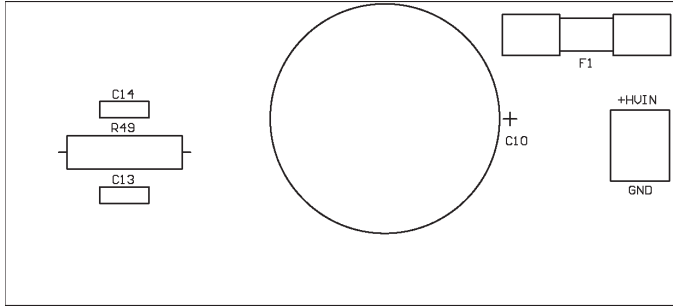


Figure 22f. Bus Power PCB Top Silkscreen

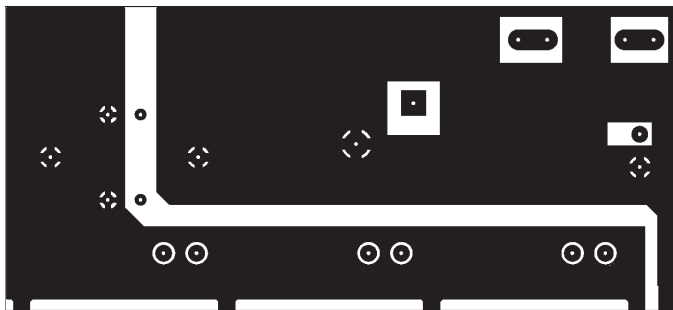


Figure 22g. Bus Power PCB Top Layer

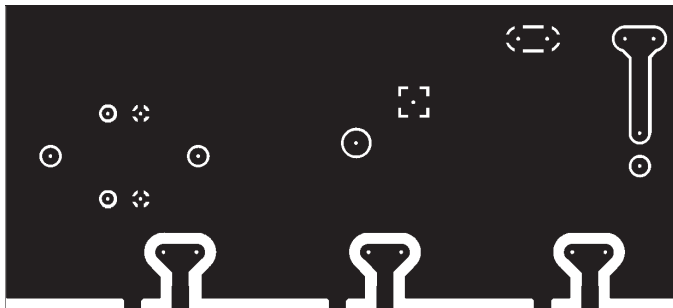


Figure 22h. Bus Power PCB Bottom Layer

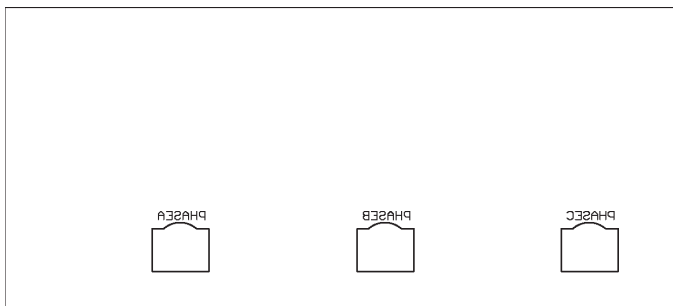


Figure 22i. Bus Power PCB Bottom Silkscreen

COMPONENT SELECTION

CAPACITORS

Since the ML4423 uses an external R/C to set up the low frequency oscillator, drift over temperature is directly related to the component tolerances at this node. If tight frequency tolerance is necessary this should be reflected in the component tolerances for the anticipated operating temperature range.

RESISTORS & CURRENT SENSE RESISTORS

For best results, use 1% resistors in the voltage feedback path. Wirewound resistors must not be used in the current feedback path. A wirewound resistor can add 200nH of circuit loop inductance, or the equivalent of a 20" long trace. With a 200ns fall time, 5A of current translates into a 5V spike across the current sense resistor for that period of time. This will trip the current limit on the ML4423 and cause problems with the bootstrap circuit and the associated level shifter.

LEVEL SHIFTERS

The ML4423 and the level shifter used to drive the upper IGBTs must provide the correct polarity signal to the IGBT or a shootthrough short circuit will occur. Some level shifters do not incorporate a pulse filter which rejects small pulse widths. This may cause the level shifter to latch in one mode and not reset. This typically occurs near the crest of the output phase waveform, so when the latch is not reset the ML4423 feedback error increases and you lose part of the output cycle. If the bootstrap cap discharges to the undervoltage lockout of the level shifter the output cycle may also drop out.

BOOTSTRAP DIODES

The diodes used for generating the bootstrap voltage must be ultra-fast (< 75ns). Slow devices will have a long recovery time and can cause dV/dt induced noise coupling problems. The diode should have at least 100V of margin over the maximum bus voltage.

POWER DEVICES

IGBTs are suited to compete with MOSFETs to 20kHz. The co-pack IGBT's have softer and faster internal diodes than MOSFETs. The relatively slow and snappy characteristics of MOSFET diodes (in freewheel mode, common for motor control) may cause chaos on ground referenced current limit schemes, and will require larger R/C filtering on the I_{SENSE} pin. EMI considerations will also play a role in device selection.

POTENTIAL DESIGN ISSUES

Other design issues to consider include: power switch size, power dissipation and heatsinking, gate drive power, gate charge, cost and reliability, and PCB layout.

COMPONENT SELECTION (Continued)

EXAMPLE: SELECTING IGBT AND HEATSINK

The following exercise selects a suitable power device and heatsink for a 1/2 HP inverter. The selected IGBT is an IRGBC20UD2. The requirements are:

- 1/2 HP 220VAC three phase induction motor
- DC input (V_{BUS}) \cong 360V DC
- motor power factor (PF) \cong 0.7
- motor efficiency (M_E) \cong 0.7
- inverter modulation index (D) = 0.612 (Eq.1, p.1)
- $f_{PWM} = 20\text{kHz}$
- Ambient Temperature $T_A = 40^\circ\text{C}$

IGBT datasheet characteristics of interest are:

- V_{CEON} @ I_C
- V_{DIODE} @ I_C
- E_{ON} @ I_C
- E_{OFF} @ I_C
- Gate charge
- θ_{JC}
- θ_{CS}

1. Calculate motor phase current required:

$$I_{PHASE} = \frac{P_{MOTOR}}{\sqrt{3} \times V_{BUS} \times Pf \times D \times M_E} \quad (5)$$

$$I_{PHASE} = \frac{\left(\frac{746\text{W}}{\text{HP}} \times 0.5\text{HP}\right)}{\sqrt{3} \times 360\text{V} \times 0.7 \times 0.612 \times 0.7} = 2\text{A}_{RMS}$$

Then peak device collector current is:

$$I_{CPK} = I_{PHASE} \times \sqrt{2} = 2.83\text{A}$$

2. Calculate IGBT conduction losses:

V_{CEON} for peak operating current \cong 2V

$$P_{ON} = I_{CPK} \times V_{CEON} \times \left(0.125 + \frac{D}{3\pi}\right) \times PF \quad (6)$$

$$P_{ON} = 2.83 \times 2\text{V} \times \left(0.125 + \frac{0.612}{3\pi}\right) \times 0.7 = 0.75\text{W}$$

3. Calculate IGBT switching losses:

E_{TOT} switching losses = 0.71mJ

$$P_{SW} = E_{TOT(mJ)} \times F_{PWM(kHz)} \times \frac{1}{\pi} \quad (7)$$

$$P_{SW} = 0.71 \times 20 \times \frac{1}{\pi} = 4.52\text{W}$$

4. Calculate diode conduction loss:

Diode voltage drop = 1.6V @ 2.83A

$$D_{COND} = I_{CPK} \times V_{DIODE} \times \left(0.125 + \frac{D}{3\pi}\right) \times PF \quad (8)$$

$$D_{COND} = 2.83 \times 1.6\text{V} \times \left(0.125 + \frac{0.612}{3\pi}\right) \times 0.7 = 0.60\text{W}$$

5. Calculate total losses:

$$T_{PD} = P_{ON} + P_{SW} + D_{COND} \quad (9)$$

$$T_{PD} = 0.75\text{W} + 4.52\text{W} + 0.6\text{W} = 5.87\text{W}$$

6. Calculate total power dissipation to select heatsink size. Total inverter losses:

$$P_{INV} = T_{PD} \times 6 \quad (10)$$

$$P_{INV} = 5.87\text{W} \times 6 = 35.22\text{W}$$

7. Calculate heatsink size with T_{SINK} selected at 125°C .

Thermal impedance is:

$$\theta_{SA} = \frac{T_{SINK} - T_A}{P_{INV}} \quad (11)$$

$$\theta_{SA} = \frac{125^\circ\text{C} - 40^\circ\text{C}}{35.22\text{W}} = 2.4^\circ\text{C} / \text{W}$$

8. Calculate IGBT and diode junction temperature for the selected T_{SINK} :

IGBT junction temperature is:

$$T_{JIGBT} = T_{SINK} + \left[(P_{ON} + P_{SW}) \times (\theta_{JC} + \theta_{CS})\right] \quad (12)$$

$$T_{JIGBT} = 125 + [(0.75 + 4.52) \times (2.1 + 0.5)] = 138.7^\circ\text{C}$$

Diode junction temperature is:

$$T_{JDIODE} = T_{SINK} + \left[D_{COND} \times (\theta_{JC} + \theta_{CS})\right] \quad (13)$$

$$T_{JDIODE} = 125 + [0.60 \times (2.1 + 0.5)] = 126.6^\circ\text{C}$$

Note: For reliable operation, T_{JIGBT} and T_{JDIODE} should be lower than 125°C ., forcing a reduction in the RQ_{SA} requirement.

9. Calculate the R_{SENSE} resistor value:

$$I_{SENSE(PEAK)} = I_{PHASE} \times \sqrt{2} \quad (14)$$

$$I_{SENSE(PEAK)} = 2\text{A} \times 1.414 = 2.83\text{A}$$

$$R_{SENSE} = \frac{0.5\text{V}}{I_{SENSE}} \quad (15)$$

Application Note 67

COMPONENT SELECTION (Continued)

$$R_{\text{SENSE}} = \frac{0.5\text{V}}{2.83\text{A}} = 0.176\Omega$$

10. Finally, calculate resistor power dissipation:

$$P_{\text{DISS}} = \left(\frac{I_{\text{SENSE(PEAK)}}}{\sqrt{2}} \right)^2 \times R_{\text{SENSE}} \quad (16)$$

$$P_{\text{DISS}} = \left(\frac{2.83\text{A}}{\sqrt{2}} \right)^2 \times 0.176\Omega = 0.7\text{W}$$

Adjustment factors have not been included for lower bus voltages.

GATE DRIVE CONSIDERATIONS

Choosing the bootstrap capacitor: The phase output referenced inverter waveforms pertain to the basic inverter design and operation. The formulas provided by IR for selecting the Bootstrap capacitor value address non-saturating PWM designs. Since the phase waveforms clip even when the differential waveforms are sinusoidal, (Figure 22) the upper switch has to stay on for the duration

without being refreshed. This requires the bootstrap capacitor to be larger than the value initially calculated. As a quick approximation, $2\mu\text{F}/\text{HP}$ works with the IR2118. For the following conditions:

- IR2118 high side gate driver
- $I_{\text{QBS}} = 50\mu\text{A}$, typical
- $V_{\text{CC}} = 12\text{V}$
- $T_{\text{ON}} = 5\text{ms}$
- IGBT gate charge = 22nC (for the IRGBC20UD2)

$$C_{\text{BOOT}} > 2 \times Q_{\text{G}} + \frac{2 \times I_{\text{QBS}} \times T_{\text{ON}}}{V_{\text{CC}} - 1.5 - 10} \quad (17)$$

$$C_{\text{BOOT}} > 2 \times 22\text{nC} + \frac{2 \times 50\mu\text{A} \times 5\text{ms}}{0.5} > 0.544\mu\text{F}$$

In this case use a $1\mu\text{F}$ capacitor.

Note: If I_{QBS} increases to $240\mu\text{A}$, $C_{\text{BOOT}} = 4.88\mu\text{F}$

Selecting the value for the series gate resistor should be based on the available peak driver current of the driver IC used. Typically, datasheet R_{G} values will work for most applications.

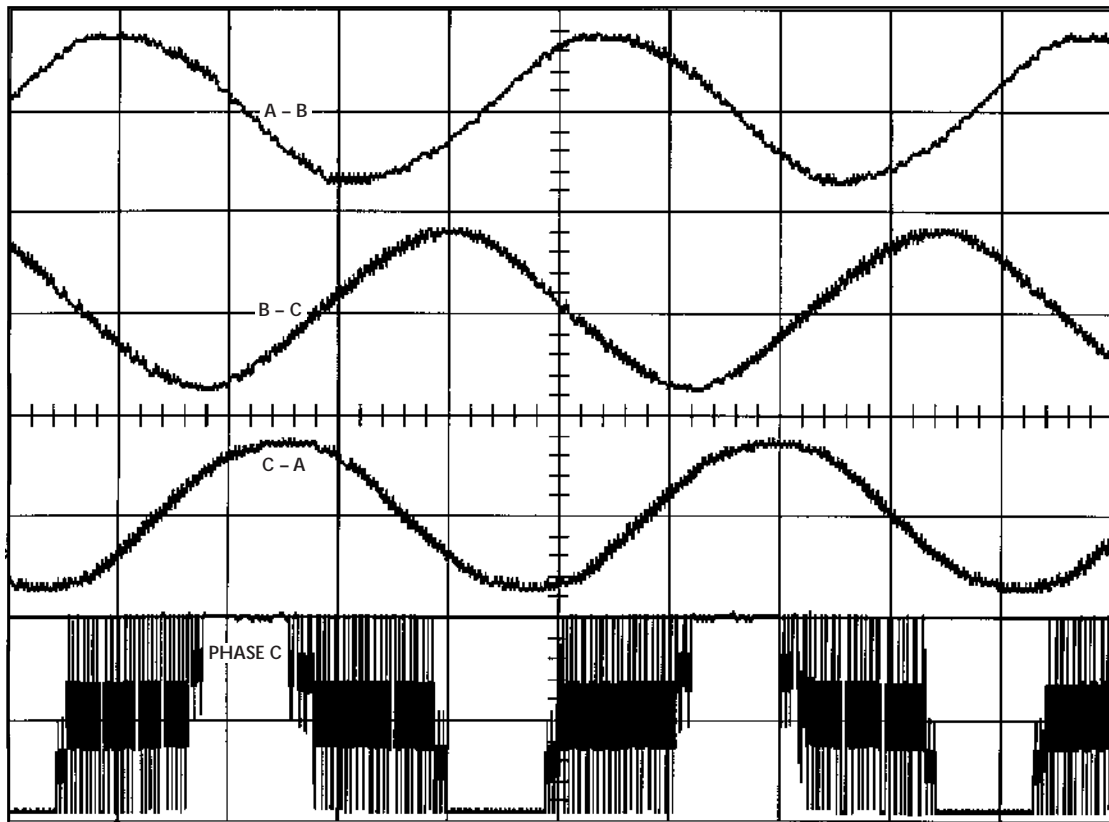


Figure 23. Clipped Phase C

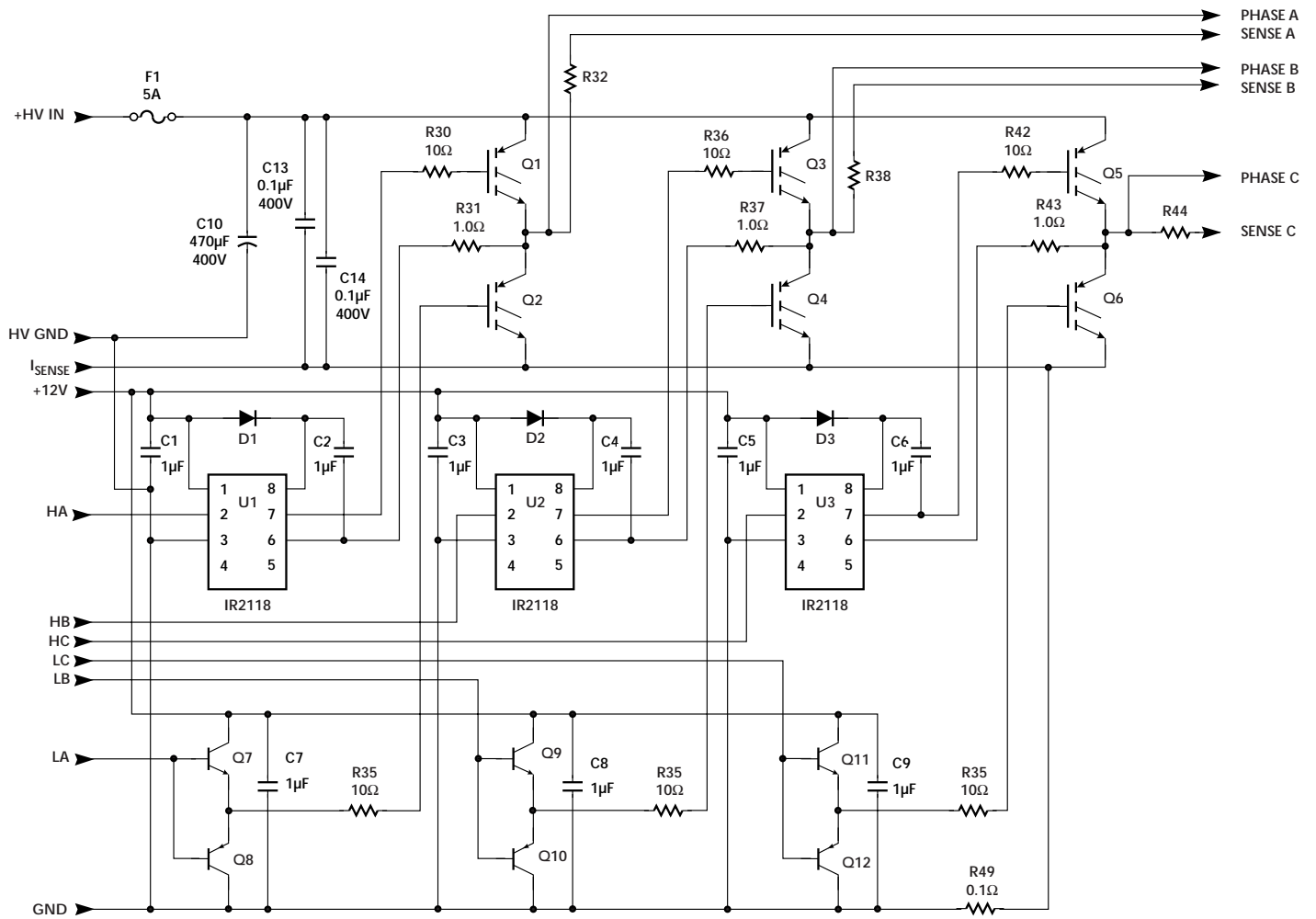


Figure 24. Inverter Schematic

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