

Thermal Considerations for Surface Mount Packages

Fairchild Semiconductor
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As package sizes continue to decrease, as well as the shift from through board to surface mount packaging, thermal considerations become increasingly important. Device life is halved for every 10°C increase in temperature. Therefore, an understanding of thermal performance becomes increasingly critical.

The following information is a brief overview of thermal properties, testing and data for surface mount packaging.

THERMAL PROPERTIES OVERVIEW

It is recommended that the junction temperature not exceed 150°C for plastic packaged devices, this is the glassification temperature (T_g). Junction temperature is a function of the power dissipation by the device, package thermal resistance, and ambient temperature outside the package.

Thermal Resistance

Thermal resistance (θ_{JA}) is a function of die and package geometries, construction and package materials, eg: die attach material, lead frame material, and mold compound; as well as the ambient air-flow, and the power dissipation of the device. It is defined as:

$$\theta_{JA} = \frac{T_J - T_A}{P} \quad (\text{°C/W}) \quad (1)$$

Where T_J is Junction temperature during power dissipation, T_A is Ambient air temperature, and P is Power dissipated by the die.

Maximum Safe Ambient Temperature

To determine the maximum ambient temperature a device can safely operate at, substitute the glassification temperature for T_J and solve for T_A maximum.

$$T_A(\text{max}) = T_G - \theta_{JA}P = 150 - \theta_{JA}P \quad (2)$$

P in this formula is based on device power for the application in which the device will be used.

THERMAL TEST SETUP AND CALCULATIONS

Thermal Test Setup

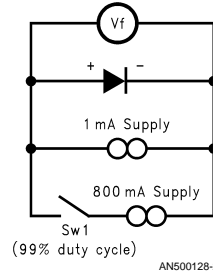
For thermal evaluation, devices or test die are heated to a specified power level via a voltage/current combination. Typically, this is accomplished by forward bias of parasitic PN junction between V_{CC} and GND. This heats the device to a specified level (Anode at ground cathode at V_{CC}).

Note: Most digital semiconductor products have parasitic PN junctions between V_{CC} and ground.

Temperature measurements are indirectly determined from the difference in forward voltage drop across the internal PN junction; the temperature is then derived from a calibrated linear equation for a particular junction current level. This is accomplished by using a low current and stepping the temperature. The calibration data is derived from the voltage change across temperature.

The die junction temperature is derived using power cycling. By using a current/voltage combination at a greater than 99% duty cycle, the PN junction is measured during the <1% time slot. In the following example a 1 mA current level vs the

800 mA level used during the 99% of duty cycle, at 1.25V this sources 1W during the 99% duty cycle, and 1mA during the <1% time



DUTs (device under test) are subjected to a myriad of environmental conditions (i.e., wind speeds, temperatures, humidity) while a known power level is applied to the device under test. Individual θ_{JA} are calculated at each of these conditions.

Thermal Test Calculations

Temperature measurements are derived from the forward voltage drop (V_f) across an internal junction at a low current level. Temperature is calculated from a calibrated linear equation for a particular current level. Temperature measurements are taken to determine the thermal resistance (θ_{JR}), as noted by the equation:

$$\theta_{JR} = (T_J - T_R) / \text{Power}$$

Where T_R is the reference temperature (i.e., ambient, case). In the case of θ_{JC} , the DUT package is mounted to a large copper heat sink while being conditioned to a predetermined temperature.

θ_{JA} tests are performed in a wind tunnel where the DUT is exposed to pre-determined environmental conditions. This is done with the device mounted on a spec'd board, which must be aligned to the laminar flow.

THERMAL TEST SETUP AND CALCULATION OUTLINE

The above discussion is laid out in outline form below:

Objective:

Find the increase in die temperature due to a given amount of dissipated heat/power.

$$\theta_{JR} = (T_H - T_R) / P \quad \text{Assume } R = \text{ambient: } \theta_{JA}$$

Where θ_{JR} is Thermal Resistance from the junction to the reference point, T_H is die Temperature after Heating with power, T_R ambient Temperature before heating, or Reference Temperature, and P is measured wattage, or Power dissipation.

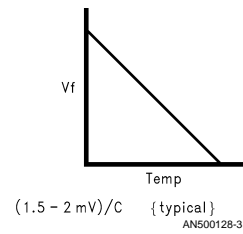
Known:	Unknown:
Die Size	Thermal Resistance
Package (composition and size)	
Power dissipation of application	

Problem:

How to determine Actual die temperature during heating; it is not accurate or convenient to place a thermocouple on the die.

Solution:

Use the linear relationship between Voltage vs Temperature for a Given Package/Die combination.



Where V_f is Voltage Forward biased through the device PN Junction and Temp is the ambient air temperature.

Implementation:

Two general approaches;

1. Thermal test die (a convenient package/die combination tool)
2. Actual product (in application { the focus here is on maximum accuracy; exact package/die/etc.})

I. Generate V vs T

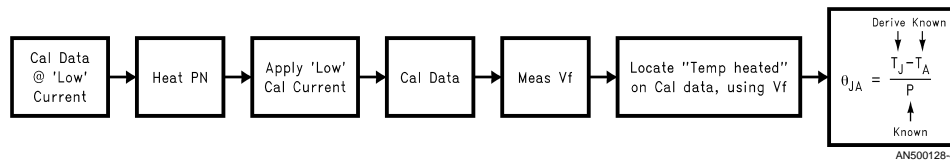
Force: ~ 1 mA at indexed temperatures {1 mA is used in order to avoid die heating}

Measure: V_f of temperature sensitive device (PN junction)

II. For each power dissipation/wind combination, measure V_f at thermal equilibrium.

III. Using the graph/table/linear equation (all are equivalent) derive the T_J .

IV. Knowing T_A , T_J , and Power, θ_{JA} is calculated.



DEVICE POWER DISSIPATION CALCULATIONS

Power dissipated in an IC is a function of the power supply voltage, input/output conditioning, output loading, operating frequency, and duty cycle. The following is intended to be a step by step approach to understanding and calculating power dissipation in semiconductor devices. Due to significant differences both inherent and designed in, the calculation section is broken into two sections, CMOS Power Dissipation, and Bipolar Power Dissipation.

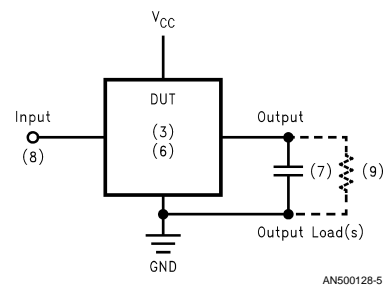
CMOS Power Dissipation

The formula for total power dissipated in a CMOS device is:

$$P = P_Q + P_{CPD} + P_{CLD} + P_{TH} + P_{ODC}$$

Where P is Total device power, P_Q is Quiescent Power, P_{CPD} is Power Dissipation Capacitance, P_{CLD} is Capacitance Load Power, P_{TH} is TTL level inputs High Power dissipation, and P_{ODC} is Power dissipation for Outputs driving a DC load.

The above formula is broken out below in steps. The diagram, with formula numbers included, is provided to illustrate the formula to device relationship:



The power dissipated in a CMOS device driving a purely capacitive load is given in the FACT data book, section one as:

$$P_Q = I_{DD} V_{DD} \quad (3)$$

Where P_Q is power dissipated during quiescent on (i.e., idle state, power on but not driving a load or running at any frequency), I_{DD} is quiescent power supply current drain, and V_{DD} is the power supply voltage.

$$P_{CPD} = f V_S V_{DD} C_{PD} \quad (4)$$

Where P_{CPD} is power dissipated via Capacitive power dissipation, f is the frequency, V_S is the output voltage swing, V_{DD} is the V_{CC} voltage, and CPD is Power Dissipation Capacitance.

$$P_{CLD} = f V_S V_{DD} C_{LD} \quad (5)$$

Where P_{CLD} is power dissipated via output load (Capacitive), f is the frequency, V_S is the output voltage swing, V_{DD} is the V_{CC} voltage, and CLD is Capacitive output load.

During device idle times, the dynamic components, equal zero. The active time duty cycle, (A_{time}), represents the percentage of time the device is active, (outputs enabled). Including the A_{time} factor, the dynamic power components and recognizing that they represent power per output pin, become:

$$P_{CPD} = N_{int(f)} f V_S V_{DD} C_{PD} A_{time} \quad (6)$$

$$P_{CLD} = N_{o(f)} f V_S V_{DD} C_{LD} A_{time} \quad (7)$$

Where $N_{int(f)}$ and $N_{o(f)}$ are the average number of internal paths, and outputs respectively, toggling at frequency (f). For gates, buffers, line drives, and transceivers, $N_{int(f)} = N_{o(f)}$.

Refer to Power Dissipation Test Philosophy in the LOGIC Applications Handbook, for the JEDEC standard on C_{PD} (device power dissipation, capacitance) measurements.

An additional term is required for CMOS parts with TTL compatible inputs (when driving the device using TTL level signals):

$$P_{TH} = N_T I_{DDT} V_{DD} D_{IH} \quad (8)$$

Where N_T is the number of the TTL compatible inputs and D_{IH} is the duty cycle inputs high.

This is critical, because at TTL high levels on the inputs, ICCT will increase dramatically, due to the fact that more of the input CMOS transistors will be on for a larger percentage of the time, greatly increasing current flow, and power consumption.

If DC loads are being driven, an additional term is required:

$$P_{ODC} = [N I_{OH} (V_{DD} - V_{OH}) D_{OH} + N I_{OL} V_{OL} D_{OL}] A_{TIME} \quad (9)$$

Where D_{OH} and D_{OL} are the duty cycles of outputs high and low (with outputs enabled), respectively. I_{OH} and I_{OL} are DC load dependant. For a capacitive load, $I_{OH} = I_{OL} = 0$. For TTL type inputs: $I_{OL} = N_i * I_{IL}$, and $I_{OH} = N_i * I_{IH}$.

Therefore, the total power dissipated in a CMOS device is the sum of (3), (6), (7), (8), and (9):

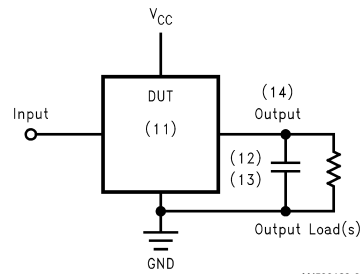
$$P = P_Q + P_{CPD} + P_{CLD} + P_{TH} + P_{ODC}$$

Bipolar Power Dissipation

The formula for total power dissipated in a Bipolar device is:

$$P = P_{OE} + P_{OH} + P_{OL} + P_{(f)} \quad (10)$$

The above formula, is broken out below in steps, the diagram with formula numbers included, is provided to illustrate the formula to device relationship:



The DC power dissipated in a bipolar device can be described in terms of the output conditioning as follows:

$$P_{OE} = I_{CCZ} V_{CC} (1 - A_{time}) \quad (11)$$

Where P_{OE} is the power dissipated during disabled time, $(1 - A_{TIME})$ represents the percent of time the device is inactive.

$$P_{OH} = [I_{CCH} V_{CC} + N I_{OH} (V_{CC} - V_{OH})] D_{OH} A_{time} \quad (12)$$

$$P_{OL} = [I_{CCL} V_{CC} + N I_{OL} (V_{CC} - V_{OL})] D_{OL} A_{time} \quad (13)$$

Where D_{OH} and D_{OL} are the duty cycles of outputs high and low (with outputs enabled), respectively. A_{TIME} is the duty cycle of the outputs enabled. I_{OH} and I_{OL} are DC load dependant. For a capacitive load, $I_{OH} = I_{OL} = 0$.

For TTL inputs, $I_{OH} = N_i * I_{IH}$, $I_{OL} = N_i * I_{IL}$. Also, since V_{OH} is dependant on V_{CC} , use $V_{OH} = (V_{CC} - 2)$ instead of the databook V_{OH} . Use databook limits for all other parameters.

The Frequency dependant component can be expressed as:

$$P_{(f)} = N_{(f)} F V_S V_{CC} (C_{PD} + C_{LD}) A_{TIME} \quad (14)$$

Where $N_{(f)}$ is the average number of outputs switching at f , (for a 16-bit count sequence, $N_{(f)} = 2$) and C_{LD} is the capacitive output load.

Therefore, the total power dissipated in a bipolar device is the sum (10), (11), (12), (13), and (14):

$$P = P_{OE} + P_{OH} + P_{OL} + P_{(f)}$$

θ_{JA} vs Air Flow, Power Derating Curves

Power derating curves can be generated by plotting power dissipated vs T_A max as a function of θ_{JA} for various airflows. The curves can be used for quickly determining maximum safe ambient temperature, and to determine if air flow is required for a given device/power level.

To use the derating curve chart to calculate power dissipation for a device; start by calculating the power that the device will dissipate under the expected conditions. Next, select the Power Derating Curves for the package being used. Locate the calculated power along the vertical axis, then drawn a horizontal line across the chart. The maximum recommended ambient temperature, for each recommended level of air flow, is the temperature where the power line intersects with the derating curve for that air flow. If the temperature where the power line intersects the zero-flow line is greater than the max operating temperature of the system, than no air flow is required.

Sample Power Derating Curves have been included for various surface mount packages and pinouts. (Appendix I) Note

that die size, technology, and package materials and packaging manufacturing methods play a crucial part in calculating derating curves.

Sample Calculations

Example 1:

Find the power dissipation and max ambient temperature for a Fairchild 74ACTQ16374, (16-bit D-Flip Flop), running at 33 MHz, 40% of the time, with TTL high inputs switching all 16 bits high to low at a 50% duty cycle during the 40% active time. The supply voltage is 5.5V and the outputs are loaded with 50 pF.

$$P_Q = I_{DD} V_{DD}$$

$$P_Q = (80 \mu A) (5.5) = 0.00044W$$

$$P_{CPD} = N_{INT(f)} f V_S V_{DD} C_{PD} A_{time}$$

$$P_{CPD} = (16) (33 \text{ MHz}) (5.5) (5.5) (30 \text{ pF}) (0.40) = 0.195W$$

$$P_{CLD} = N_{O(f)} f V_S V_{DD} C_{PD} A_{time}$$

$$P_{CLD} = (16) \left(\frac{33}{2} \text{ MHz} \right) (5.5) (5.5) (50 \text{ pF}) (0.40) = 0.160W$$

Note: In this example the outputs toggle at one half the clock frequency, as the 74ACTQ16374 is a D type flip flop.

$$P_{TH} = N_T I_{DDT} V_{DD} D_{IH}$$

$$P_{TH} = (16) (1.5 \text{ mA}) (5.5) (0.5) = 0.066W$$

$$P = P_Q + P_{CPD} + P_{CLD} + P_{TH} + P_{ODC}$$

$$P = (0.00044W) + (0.195W) + (0.160W) + (0.066W) + (0) = 0.42W$$

Checking the power derating chart for 48-lead SSOP shows that temperatures of greater than 90°C can be supported with no air flow at this power level.

Example 2:

Find the power dissipation and maximum ambient air temperature for a Fairchild 74FR16245 (16-bit transceiver with 3-state outputs), running at 33 MHz, 50% of the time, with all 16 inputs switching randomly. The supply voltage is 5.0V and the outputs are loaded with 10 Fast unit loads each. (Unit load = $I_{IH} = 20 \mu A$, $I_{IL} = 0.6 \text{ mA}$, $C = 4.5 \text{ pF}$).

For 16 inputs switching randomly, $D_{OH} = D_{OL} = 0.5 N(f)$ can be found by multiplying the number of inputs by the probability of an input switching:

$$N(f) = N \Psi \left(\frac{1}{f} \right) = (16) (0.5) = 8$$

The average power dissipation by the transceiver is:

$$P_{OE} = I_{CCZ} V_{CC} (I-A_{time})$$

$$P_{OE} = (105 \text{ mA}) (5.0) (1 - (0.5)) = 0.262W$$

$$P_{OH} = [I_{CCH} V_{CC} + N I_{OH} (V_{CC} - V_{OH})] D_{OH} A_{time}$$

$$P_{OH} = [(105 \text{ mA}) (5.0) + (16) (.2 \text{ mA}) ((5.0) - (3))] (0.5) (0.5) = 0.133W$$

$$P_{OL} = [I_{CCL} V_{CC} + N I_{OL} (V_{CC} - V_{OL})] D_{OL} A_{time}$$

$$P_{OL} = [(165 \text{ mA}) (5.0) + (16) (6 \text{ mA}) (0.55)] (0.5)(0.5) = 0.219W$$

$$P_{(f)} = N(f) F V_S V_{CC} (C_{PD} + C_{LD}) A_{TIME}$$

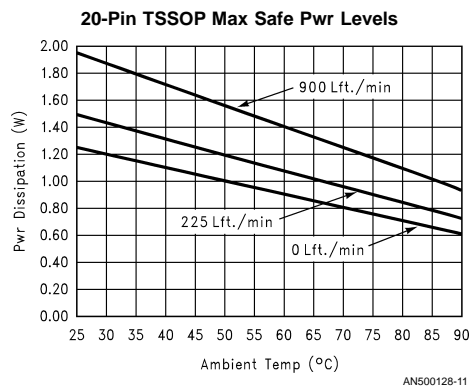
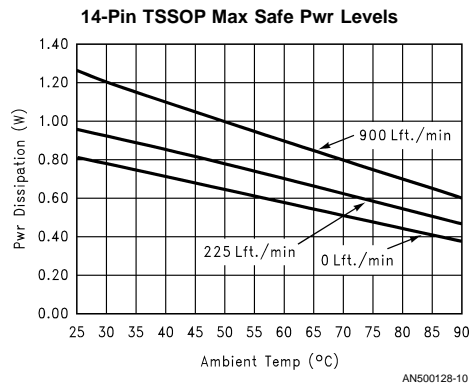
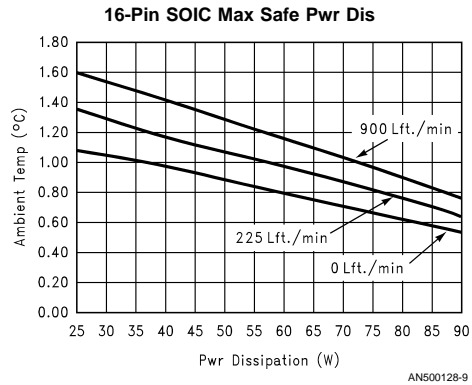
$$P_{(f)} = (8) (33 \text{ MHz}) (3.0) (5.0) ((18 \text{ pF}) + (4.5 \text{ pF} * 10)) (0.5) = 0.125W$$

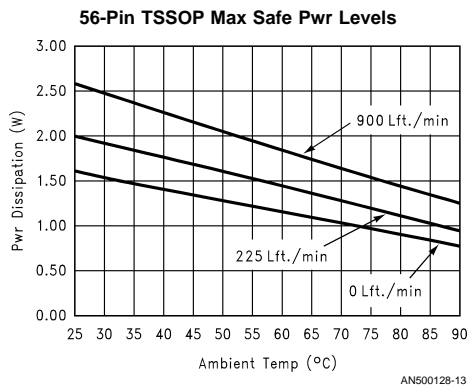
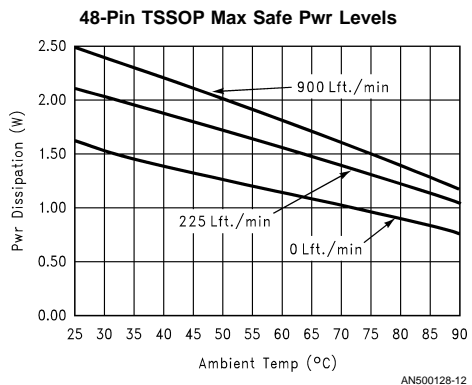
Therefore, the total power dissipated in this example is:

$$P = P_{OE} + P_{OH} + P_{OL} + P_{(f)}$$

$$P = (0.262W) + (0.133W) + (0.219W) + (0.125W) = 0.739W$$

Checking the power derating chart for 48-lead SSOP shows that the maximum ambient temperature for safe operation with no airflow for the above equation conditions is 90°C.





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